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A METHOD OF THE SCAN CHECKING FOR ON-LINE TESTING OF SAFE MULTITHREADED BITWISE PIPELINE SYSTEM

On the basis of resource approach, prospects in development of computer system components and their on-line testing in the natural path of increasing a level of parallelism and fuzziness are considered. Disadvantages of matrix parallelism are marked, and transition to safe multithreaded bitwise pipeline processing of data is reasoned. The method of the scan checking for safe multithreaded system of the bitwise pipelines in approximate data processing is offered. Reliability of the method increases by domination in detection of essential errors caused by faults of circuits in most significant bits of results.

Key words: *on-line testing; resource approach; safety, model of approximate data; multithreaded bitwise pipeline processing of data; scan checking method; reliability.*

Introduction

According to resource approach, matrix and pipeline types of parallelism belong to replication and diversification which occupy respectively the low and middle level in development of resources: models, methods and means [1]. Level of diversification stimulates development of the resource features increasing trustworthiness of results and safety of critical infrastructures [2].

The modern computer systems and their digital components are built in the form of the pipeline. However sections of the pipeline are single-cycle matrix units (parallel adders and shifters, iterative array multipliers and dividers). They receive input data represented in parallel codes. However these codes will be processed sequentially from the low-order bit to the high-order bit.

The structure of the fastest circuit of the iterative array multiplier contains $2N-2$ sequentially of connected operational elements (full adders) where N – size of an operand [3, 4], i.e. each of almost N^2 of operational elements is used in clock cycle with coefficient $K_U = (2N-2)^{-1}$. In case of $N = 32$, the operating time of each of 10^3 operational elements makes $K_U = 1.6\%$ and there are less than one percent with transition to a 64-bit platform.

Digital circuits of matrix units have a low checkability which is one of the reasons generating a problem of the hidden faults in safety-related instrumentation and control systems ensuring the functional safety in objects of the increased risk [5]. These systems are designed for operation in two modes: normal and emergency. The problem of the hidden faults consists in accumulation of faults which are hidden in a normal mode of digital circuits and reduce their fault tolerance and safety of system in emergency mode [6].

Besides, propagation of signals in matrix units is followed by critical races with waves of parasitic transitions (switching). It in addition increases energy consumption of digital circuits. It is known, that 8-b ripple-carry adder with uniformly distributed set of random input pattern will typically consume an extra 30% in energy [7]. Research of the iterative array multiplier on program model shows that execution of one multiplication changes values of signals in 30% of the digital circuit points. This necessary number of transitions increases more than by 3 times for the 8-b multiplier and grows for 50% with increase in the size of an operand by two bits.

Reduction of a share of matrix parallelism up to one operational element in section is important reason in favor of transition to the bitwise pipelining significantly raising a ratio of productivity / complexity. In this case, support of high throughput requires transition to the multithreaded organization of computation.

The bitwise pipeline processes data in sequential codes, increasing a level of parallelism: all bits will be processed at the same time on different sections of the pipeline. Complexity of the arithmetical unit decreases from square dependence on the size of operands to the linear.

Data processing in sequential codes will transform registers of operands to scan registers which are elements of testable design [8]. It raises a checkability of the digital circuit and aligns it for the normal and emergency modes of system. The faults reducing fault tolerance of the digital circuit in emergency mode lose the hidden character in a normal mode. The hidden faults aren't shown in emergency mode. It solves a problem of the hidden faults in safety-related systems [9].

Alignment of propagation delays of signals

eliminates losses of energy on critical races. Besides, bitwise piping repeatedly reduces quantity of inputs and outputs of arithmetical units. It raises a level of their self-sufficiency (independence of external nodes) in the path to the top level of resource development – autonomy [1, 10].

The described development of computer systems requires the appropriate enhancement of their on-line testing methods playing an important role in safety-related systems [11, 12]. Thus, development of on-line testing methods for multithreaded bitwise pipeline system becomes pressing problem.

Resources develop from simple to real by structuring under features of the natural world. Simple forms are exact and sequential according to initial opportunities and representations of the person. Real resources reflect features of the natural world. History of development of computer resources most brightly showed two such features: parallelism and fuzziness.

The model of number passed a way from exact data, i.e. integer by the nature, to the approximate form parallelized to the two-component representation in floating-point formats as the product $m\,B^E$ where m – a mantissa, E – an exponent in case of the fixed base B of numeration systems [13].

The model of computing operation, since the level of matrix parallelism, gained development in the truncated form [14, 15] with single precision when the result inherits the operand size (homogeneous floating-point operations) [16].

The model of approximate data distinguishes most significant bits (MSB) and least significant bits (LSB) [17]. Faults of circuits cause in these bits the errors which are respectively essential and inessential for trustworthiness of results. The on-line testing method reliability determined by the amount of probabilities in detection of essential errors and skipping of inessential ones, increases in case of the best detection of essential errors in comparison with inessential [18].

The analysis of on-line testing methods for approximate calculations shows that the scan checking developed for array units takes into account their structure regularity, typical also of multithreaded bitwise pipeline system [19].

Therefore this paper is devoted to development of the method of scan checking with the domination in detection of essential errors in the results calculated in case of multithreaded data processing with bitwise pipelining of calculations. In section 1 the domination problem in detection of essential errors in the bitwise pipeline is defined. The solution for data processing, starting with low orders is proposed. In section 2 different options of the organization of check calculations for domination in detection of essential errors are considered. Reliability of the offered method is estimated in section 3.

1. Scan checking of bitwise pipeline

The scan checking enters into a multithreaded system the additional bitwise pipeline which in turn will be connected to inputs of the main pipelines of system for calculation of test results in parallel with the main ones.

Comparing of the main and test results allows to estimate their trustworthiness. The dominating in detection of essential errors can be provided by verification of high orders of results more often than low orders. Traditionally data handling begins with low orders. In this case, verification of several high orders requires execution of all arithmetical operation in the additional pipeline. Checking of low orders shall be locked for reduction in the frequency of their check.

We offer a method of the scanning checking of system of bitwise pipelines which checks high orders of result with minimum loss of time for lock of checks. The additional pipeline executes abridged operation. Computation begins with clock cycle which guarantees the minimum difference of the checked bits in the main and test results. This difference shan't exceed weight of the low position in checked bits. Comparing of high orders of results is executed to within weight of this position. The clock cycle of connection of the additional pipeline to the main one coincides with clock cycle of the beginning of comparing of high orders in checking of addition in sequential code. Really values of the main and test results differ only on value of carry from low orders. For other operations, the difference Δ of clock cycle numbers shall be calculated.

Calculation of difference Δ for multiplication of n-bit binary codes $X\{1 \div N\}$ and $Y\{1 \div N\}$ is based on the analysis of an Array of Product Conjunctions (APC) which is shown in fig. 1 for n = 8.

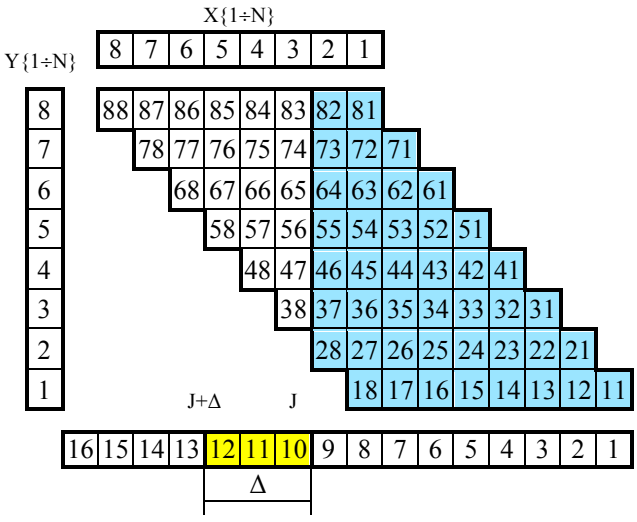

Fig. 1. Array of product conjunctions

Let J – number of clock cycle from which the additional pipeline begins to execute abridged operation of multiplication, $N-\Delta \le J \le 2N-\Delta$. Columns of high part of the APC begin with this number. The offered method checks high orders with numbers from $J+\Delta$ to $2N$ by comparing of their values in main and test results. These bits will be considered authentic if their difference doesn't exceed weight $2^{J+\Delta-1}$ of bit $J+\Delta$.

Let M, M_H and M_L – values of the APC, its high and low part when all their conjunctions are equal to unit; $M=M_H+M_L$. Value M_L corresponds to a worst case situation when the low part of the APC is ignored in calculation of abridged product in the additional pipeline.

Theorem. High orders $J+\Delta \div 2N$ will be checked in case of calculation of the test result, since bit J where $\Delta=\log_2 N$, i.e.

$$M_L < 2^{J+\Delta-1} = 2^{J-1} N. \qquad (1)$$

Proof. We will consider two cases: L and H.

L: $N-\Delta \le J \le N$. The low part of the APC has triangular shape, and its value is calculated as $M_L = 2^{J-1}(J-2)+1$. The condition (1) is satisfied in case of the minimum value $\Delta=\log_2(N-1)$.

H: $N \le J \le 2N-\Delta$. The high part of the APC has triangular shape. Value of low part is defined as $M_L = M - M_H$, where $M=\left(2^N-1\right)^2$, $M_H = 2^{2N} - 2^J(2N-J)$, or

$$M_L = 2^J(2N-J+2) - 2^{N+1} + 1. \qquad (2)$$

The condition (1) takes a form

$$2^J(2N-J+2) - 2^{N+1} + 1 < 2^J N. \qquad (3)$$

The proof for a case of H is executed by a method of a mathematical induction.

The condition (3) is satisfied for $J=N$ in case of L.

For the following value $J+1$ condition (3) will be transformed to a look:

$$M_L = 2^{J+1}(2N-J+1) - 2^{N+1} + 1 < 2^{J+1} N. \qquad (4)$$

The condition (4) is compared to a condition (3) in which the left and right parts double:

$$2^{J+1}(2N-J+2) - 2^{N+2} + 2 < 2^{J+1} N. \qquad (5)$$

Comparing shows that the left part of a condition (5) exceeds the left part of a condition (4) on expression $2^{J+1} - 2^{N+1} + 1 > 0$ as $N \le J$.

In case of $\Delta < \log_2 N$ the condition (3) is violated.

The proof is finished.

Thus, high orders $J+\Delta \div 2N$ of result will be checked in case of computation of $J \div 2N$ bits of abridged product, i.e. in case of use of $\log_2 N$ additional clock cycles.

2. Organization of check calculations

The organization of check calculations determines sequence of checking of the result bits.

The additional pipeline shall execute check of two types: all bits of the main result and only its high orders. In the first case the additional pipeline matches the main, and in the second case expands basic functions. Therefore the additional pipeline can be realized for sequential execution of two types of checking or execute them in parallel, using the complete pipeline identical to the main, and the simplified pipeline for checking of high orders.

The main requirement to the organization of check calculations is their recurrence which simplifies control in the checking.

Alternation of two types of checking in case of their sequential execution allows to use checking of high orders to go to checking of the following main pipeline. Execution of two types of checking in parallel shall exclude simultaneous check of the same bits of result in the complete and simplified pipeline. Transition of the complete pipeline from checking of one main pipeline to another is executed with a pause as flows of input data arrive with time offset.

The organization of computation can be considered on the example of multithreaded system of bitwise pipelines for multiplication of 16-b mantissas with use of the truncated operation. On an input of system 4 continuous data streams with offset on 4 clock cycles between adjacent flows arrive. Each mantissa arrives during sixteen clock cycles. The input switch redistributes input flows on 5 flows arriving on inputs of five main pipelines executing an truncated multiplication. They calculate 20-b truncated product of mantissas. The output switch redistributes 5 continuous flows of truncated products in 4 continuous flows of the rounded 16-b results which are given for an output of system.

The difference $\Delta=4$ allows to check 4, 8 and 12 high orders, calculating 8, 12 and 16 high orders of truncated product in the additional pipeline. All 16 bits of the rounded result are checked in case of calculation of all 20 bits of truncated product of mantissas.

The cycle of check calculation can be described by sequence of the elements specifying number of the checked main pipeline and amount of clock cycles of its connection to the additional pipeline. The element can also specify amount of clock cycles of a pause in checking. Elements separate by the character "-" from each other. Number of the checked pipeline separates by a point.

Cycles of check calculation for cases of checking of 4, 8 and 12 high orders have the following descriptions:

1.20-3.8-3.20-5.8-5.20-2.8-2.20-4.8-4.20-1.8
1.20-4.12-4.20-2.12-2.20-5.12-5.20-3.12-3.20-1.12 (6)
1.20-5.16-5.20-4.16-4.20-3.16-3.20-2.16-2.20-1.16

Number of the following checked main pipeline is calculated as

$$(F+G/\Delta)\bmod 5, \quad (7)$$

where G – amount of clock cycles of its connection to the additional pipeline;

F – number of the previous checked main pipeline.

In case of parallel execution of two types of checking, the cycle of check calculation for the complete pipeline is described by the following sequence of elements:

1.20-4-2.20-4-3.20-4-4.20-4-5.20-4, (8)

where the pause in 4 clock cycles necessary to go to checking of the following pipeline is specified.

According to a formula (7), 3 versions of the simplified pipeline connection are possible for $G=12$:

8-2.12-5.12-3.12-1.12-4.12
12-3.12-1.12-4.12-2.12-5.12 (9)
16-4.12-2.12-5.12-3.12-1.12

The first two versions exclude check of the same bits along with the complete pipeline. The last version violates this requirement in every second connection.

3. Reliability of a method

As a rule, on-line testing methods of arithmetical operations are compared to residue checking which gained the greatest distribution within model of exact data [20, 21]. However this method doesn't distinguish essential and inessential errors. It considerably reduces its reliability in on-line testing of approximate calculations.

Reliability of on-line testing methods is estimated by the following formula [22]:

$$R=P_E P_D+(1-P_E)(1-P_D), \quad (10)$$

where P_E – probability of an essential error;

P_D – probability of detection of an error.

Residue checking by modulo three reveals all errors caused by typical faults of the iterative array multiplier: $P_D=1$. Approximate calculations reduce probability of an essential error in operations of multiplication, a denormalization of operands and normalization of results to the level $P_E<0.5$. According to the formula (10), reliability of a method of residue checking is estimated as $R_R=P_E<0.5$.

Reliability of the scan checking in case of identical detection probability of essential and inessential errors is determined by the formula (10) where the probability of error detection is evaluated by the check frequency of each main pipeline: $P_D=1/M$, M is the number of the main pipelines of system. For $P_E=0.3$ and $M=4$, reliability $R=0.6$ of the scan checking method increases twice in comparison with R_R.

In case of the scan checking with different detection probabilities P_{D-E} and P_{D-I} of essential and inessential errors, reliability is estimated by the following formula [22]:

$$R_S=P_E P_{D-E}+(1-P_E)(1-P_{D-I}). \quad (11)$$

Detection probabilities of essential and inessential errors are evaluated as

$$P_{D-E}=Z_{D-E}/Z; \quad (12)$$

$$P_{D-I}=Z_{D-I}/Z, \quad (13)$$

where Z_{D-E} and Z_{D-I} – amount of clock cycles of check of MSB and LSB in a check cycle;

Z – amount of clock cycles in a check cycle.

Let the result contain identical quantity of MSB and LSB.

For example, the cycle of check (6) contains $Z=160$ clock cycles, including $Z_{D-E}=80$ and $Z_{D-I}=40$. According to the formulas (11), (12) and (13), probabilities of $P_{D-E}=0.5$ and $P_{D-I}=0.25$ determine reliability as $R_{S1}=0.675$.

Cycles of check (8) and (9) contain $Z=120$ and $Z=72$ clock cycles, respectively. The general check cycle $Z=360$ clock cycles includes $Z_{D-E}=320$ and $Z_{D-I}=120$. Probabilities $P_{D-E}=0.89$ and $P_{D-I}=0.33$ determine reliability as $R_{S2}=0.733$.

We will estimate high values of reliability by its approximation to unit. In the examined cases, increase of reliability is estimated as $K_I=(1-R_S)/(1-R_{SI})$, where $I=1$ or $I=2$, $K_1=1.2$, $K_2=1.5$.

Functionality of the offered method was confirmed experimentally during preparation of lab classes within execution of the project TEMPUS GREENCO "Green Computing & Communications" (530270-TEMPUS-1-2012-1-UK-TEMPUS-JPCR) [23].

Conclusion

Development of models, methods and means in the path of increasing a level of parallelism and fuzziness enhances our understandings of efficiency and safety of computer systems and their components. Drawbacks of matrix parallelism require development of the modern pipeline systems in the direction of multithreaded bitwise data processing in sequential codes. Such decision raises a ratio throughput / complexity, eliminates energy losses on critical races of signals, and extends possibilities of on-line testing restricted by a problem of the hidden faults in safety-related systems.

On-line testing of multithreaded system of bitwise pipelines should be developed within model of approximate data with distinguishing of the essential and inessential errors caused by faults of circuits in MSB and LSB of computed results.

The offered method of the scan checking takes structure of multithreaded system into account and detects essential errors more likely, than inessential errors by more frequent verifications of high orders. It considerably improves reliability of on-line testing methods in approximate calculations.

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МЕТОД СКАНИРУЮЩЕГО КОНТРОЛЯ ДЛЯ РАБОЧЕГО ДИАГНОСТИРОВАНИЯ МНОГОПОТОЧНОЙ ПОРАЗРЯДНОЙ КОНВЕЙЕРНОЙ СИСТЕМЫ

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На основе ресурсного подхода рассматриваются перспективы развития компонентов компьютерных систем и их рабочего диагностирования по естественному пути повышения уровня параллелизма и приближенности. Отмечаются недостатки матричного параллелизма, и обосновывается переход к безопасной многопоточной поразрядной конвейерной обработке данных. Предлагается метод сканирующего контроля для многопоточной системы поразрядных конвейеров, выполняющих обработку приближенных данных. Достоверность метода повышается за счет доминирования в обнаружении существенных ошибок, которые вызываются неисправностями схем в старших разрядах результатов.

Ключевые слова: рабочее диагностирование; ресурсный подход; функциональная безопасность, модель приближенных данных; многопоточная поразрядная обработка данных; метод сканирующего контроля; достоверность.

МЕТОД СКАНУЮЧОГО КОНТРОЛЮ ДЛЯ РОБОЧОГО ДІАГНОСТУВАННЯ БАГАТОПОТОЧНОЇ ПОРОЗРЯДНОЇ КОНВЕЄРНОЇ СИСТЕМИ

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На основі ресурсного підходу розглядаються перспективи розвитку компонентів комп'ютерних систем та їхнього робочого діагностування за природним шляхом підвищення рівня паралелізму та наближеності. Відмічаються недоліки матричного паралелізму, та обґрунтовується перехід до безпечної багатопоточної порозрядної конвеєрної обробки даних. Пропонується метод скануючого контролю для багатопоточної системи порозрядних конвеєрів, що виконують обробку наближених даних. Достовірність метода підвищується за рахунок домінування у виявленні суттєвих помилок, які викликаються несправностями схем у старших розрядах результатів.

Ключові слова: робоче діагностування; ресурсний підхід; функціональна безпека, модель наближених даних; багатопоточна порозрядна обробка даних; метод скануючого контролю; достовірність.

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